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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,298	12/31/2003	Peter Hazucha	INTEL-0057	8425

34610 7590 10/27/2005

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/748,298	HAZUCHA ET AL.
	Examiner	Art Unit
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10,12-14,17-27 and 31-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-10,12-14 and 17-27* is/are allowed.

6)☒ Claim(s) *31,34,35,37-39,42,44,46,48,50 and 51* is/are rejected.

7)☒ Claim(s) *32,33,36,40,41,43,45,47 and 49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 5-10, 12-14, 17-27 and 31-51 are presented in the instant application according to the Applicants' amendment filing on 09/07/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 31, 34, 35, 37-39, 42, 44, 46, 48 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (U.S. Patent No. 6,940,326).

With respect to claims 31, 42, 46 and 50, Chen et al. discloses, in Fig. 3, a circuit and its corresponding method, the circuit comprising a first delay line [first delay circuit] to delay a clock signal [Input] by a first amount of time; a second delay line [second delay circuit] to delay the clock signal by a second amount of time; and a signal processor [34] to generate a) a first timing signal [output from first delay circuit] from the clock signal [Input], b) a second timing signal [top output of 34] having edge transitions controlled by the first timing signal at times determined by a logical combination of the delayed clock signals from the first and second delay

lines and c) a third timing signal [bottom output of 34] having edge transitions controlled by the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines.

With respect to claim 34, Chen et al. discloses, in Fig. 3, that the signal processor includes a first logical circuit [top NOR circuit] to control the edge transitions of the second timing signal based on logical values of the first timing signal at times determined by a logical combination of the delayed clock signals.

With respect to claims 35, 44 and 48, Chen et al. discloses, in Fig. 3, that the first logical circuit [top NOR circuit] controls the edge transitions of the second timing signal based on logical values of the first timing signal at times when the delayed clock signals have a same logical value.

With respect to claim 37, Chen et al. discloses, in Fig. 3, a second logical circuit [bottom NOR circuit] to control the edge transitions of the third timing signal [output of bottom NOR circuit] based on logical values of the second timing signal at times determined by one of the delayed clock signals from the first and second delay lines.

With respect to claim 38, Chen et al. discloses, in Fig. 3, a different one of the delayed clock signals determines when the second logical circuit [bottom NOR circuit] controls the edge transitions of the third timing signal at different times.

With respect to claim 39, Chen et al. discloses, in Fig. 3, the second timing signal determines which one of the delayed clock signals controls when the second logical circuit [bottom NOR circuit] sets the edge transitions of the third timing signal based on logical values of the second timing signal [output of top NOR circuit].

Allowable Subject Matter

3. Claims 5-10, 12-14, and 17-27 are allowed.

4. Claims 32-33, 36, 40-41, 43, 45, 47 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A circuit, in which the interim timing signal has a period which is substantially twice as long as the period of the clock signal, in combination with the remaining claimed limitations, as called for in claim 5;

b) A signal processing method including a step of generating a timing signal from the interim timing signal, in which the interim timing signal is periodic with a period which is substantially twice as long as the period of the clock signal, in combination with the remaining claimed limitations, as called for in claim 12;

e) A circuit, in which a timing circuit to control input of a voltage signal through a switch, and a signal processor to generate a timing signal and different portions of the timing signal independently control input of the voltage signal though the switch, as called for in independent claim 21; and

f) A method including a step of controlling input of a voltage signal into a level converter based on a timing signal, in which different portions of the timing signal independently control switching of the voltage signal into the level converter, as called for in independent claim 24.

g) A circuit, in which the first timing signal has a period which is a number of times longer than the clock signal, as called for in claims 32, 43 and 47;

h) A circuit, in which the first logical circuit includes a data input coupled to receive the first timing signal and a clock input coupled to receive a signal indicative of a logical combination of the delayed clock signals, as called for in claim 36;

i) A circuit, in which the second logical circuit includes a data input coupled to receive the second timing signal and a clock input coupled to a multiplexer, the multiplexer selecting for output one of the delayed clock signals based oh a logical value of the second timing signal, as called for in claim 40;

j) A circuit including a controller to change at least one of the first and second amounts of time in the delay lines, to adjust a position of at least one of the first and second edges of the third timing signal, as called for in claim 41; and

k) A circuit, in which the second timing signal determines which one of the delayed clock signals controls when the second circuit sets an edge transition of the third timing signal, as called for in claims 45 and 49.

Remarks

6. Applicant is noted that newly added claim 51 depending on canceled claim 28, therefore claim 51 is not given patentable weight.

7. Applicant's remarks regarding newly added claims filed 09/07/2005 have been considered.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER